Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	32	controller with hysteresis$4 with voltag$4 with level	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:15
S5	123	microprocessor with input with threshold with compar$4 with signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/16 09:53
S10	6	microprocessor with hysteresis$4 with voltag$4 with level	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/09/19 09:13
S11	17	microprocessor with hysteresis$4 with voltag$4 with compar$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/09 13:16
S14	16	circuit with hysteresis$4 with voltag$4 with port$4 with level	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/09 13:49
S15	18	circuit with hysteresis$4 with threshold with voltag$4 with port$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/09 14:45
S16	273	circuit with hysteresis$4 with threshold with voltag$4 with compar$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/09 14:45
S21	35	circuit with hysteresis$4 with threshold with voltag$4 with compar$4 and (processor or cpu)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/09 14:46